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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/875,501
Filing Date ..... June 4, 2001
Inventor ..... Klaus Florian Schuegraf et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2815
Examiner ..... E. Ortiz
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect Structures

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether the submitted references are prior art. A copy of the references is attached.

The materials cited are presented to assist in and expedite examination of this application. The present invention is considered to be patentable over the cited materials. Expeditious examination and allowance of this application as a patent are therefore urged in order that the public may benefit from the disclosure and commercialization of the invention.

Respectfully Submitted:

Dated: 7-8-02

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